THE HONORABLE JAMES L. ROBART

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

MICROSOFT CORPORATION, a
Washington corporation,

                          Plaintiff,

       v.

MOTOROLA, INC., and MOTOROLA
MOBILITY, INC., and GENERAL
INSTRUMENT CORPORATION,

                          Defendants.

MOTOROLA MOBILITY, INC., and
GENERAL INSTRUMENT
CORPORATION,

       Plaintiffs/Counterclaim Defendant,

       v.

MICROSOFT CORPORATION,

       Defendant/Counterclaim Plaintiff.

CASE NO. C10-1823-JLR

MOTOROLA'S OPPOSITION TO
MICROSOFT CORPORATION'S
MOTION FOR SUMMARY JUDGMENT
OF INVALIDITY

**NOTED ON MOTION CALENDAR:
Friday, April 13, 2012**

ORAL ARGUMENT REQUESTED

MOTOROLA'S OPPOSITION TO MICROSOFT'S
MOTION FOR SUMMARY JUDGMENT OF
INVALIDITY
CASE NO. C10-1823-JLR

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MOTOROLA'S OPPOSITION TO MICROSOFT'S
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I.   INTRODUCTION

Motorola Mobility, Inc. and General Instrument Corporation ("Motorola") respectfully request that the Court deny Microsoft Corporation's ("Microsoft") motion for summary judgment of invalidity of claim 14 of U.S. Patent No. 7,310,374 ("the '374 patent"), claim 13 of U.S. Patent No. 7,310,375 ("the '375 patent"), and claim 22 of U.S. Patent No. 7,310,376 ("the '376 patent") (collectively "the Motorola Patents") because each of these claims meets the "definiteness" requirement of 35 U.S.C. § 112, ¶ 6 and § 112, ¶ 2.

The claims at issue are definite because the term "decoder" disclosed in the specification of the Motorola Patents is a discrete class of known structures that will perform the functions recited in those claims. The claimed functions are variations of well-known decoder functions, and one of ordinary skill in the art, reading the specification, would have known and readily understood how to modify the structure of a decoder to perform the claimed functions. Accordingly, the details of those modifications need not be disclosed in the patent specification.

Microsoft's argument that the structure corresponding to the claimed functions are required to be algorithms disclosed in the specification is misplaced because that principle applies when the only structure disclosed and claimed is a general purpose computer programmed to perform a function, which is not the case here. Even if this Court finds that the "decoder" is a general purpose computer (it is not) a person of ordinary skill in the art would understand that the Motorola patents disclose algorithms for performing the claimed functions, so summary judgment of indefiniteness must be denied.

II.   STATEMENT OF LAW

To succeed on their motion for partial summary judgment, Microsoft must show "that there is no genuine issue as to any material fact and that the moving party is entitled to judgment as a matter of law." *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 247-48 (1986) (citing to Fed. R. Civ. P. 56(c)). Even where Microsoft and Motorola draw different inferences from the same facts, "[t]he evidence of the non-movant is to be believed, and all justifiable inferences are to be

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1 drawn in his favor." *Anderson*, 477 U.S. at 255.

2 A patent is presumed valid, and the burden of establishing invalidity as to any claim of a

3 patent rests upon the party asserting such invalidity. 35 U.S.C. § 282. Clear and convincing

4 evidence is required to invalidate a patent. *See TypeRight Keyboard Corp. v. Microsoft Corp.*, 374

5 F.3d 1151, 1157 (Fed. Cir. 2004). A challenge to a claim containing a means-plus-function

6 limitation as lacking structural support, requires a finding, by clear and convincing evidence, that

7 the specification lacks adequate disclosure of structure sufficient to be understood by one skilled

8 in the art as able to perform the recited functions. *Intel Corp. v. VIA Techs. Inc.*, 319 F.3d 1357,

9 1365-66 (Fed. Cir. 2003).

10 The proper test for meeting the definiteness requirement under 35 U.S.C. § 112, ¶ 6 is that

11 the corresponding structure of a means-plus-function limitation must be disclosed in the

12 specification itself in a way that one skilled in the art will understand what structure will perform

13 the recited function. *Atmel Corp. v. Info. Storage Devices, Inc.*, 198 F.3d 1374, 1381 (Fed. Cir.

14 1999).

15 In this case, the specification of the Motorola Patents adequately discloses to one of

16 ordinary skill in the art that a "decoder" is the structure corresponding to the functions of the

17 "means for decoding" and "means for using" claims elements.[1]

18 **III.   ARGUMENT**

19 **A.   The Specification's Disclosure of a "Decoder" Is Sufficient to Indicate to a
        Person of Ordinary Skill in the Art the Structure Corresponding to the**
20 **"Means For Decoding" and "Means For Using" Claim Elements.**

21 A person of ordinary skill in the art, reading the common specification of the Motorola

22 Patents, would understand that the Motorola Patents teach using a decoder to perform the

23 functions in claim 14 of the '374 patent, claim 13 of the '375 patent, and claim 22 of the '376

24

25 [1]   The parties agreed on the eve of the *Markman* Hearing that the structure corresponding to the "means for
        decoding…" and "means for using…" claim elements is a "decoder," subject to each party reserving its position as to
26 whether structure is adequately disclosed in the specification. *See Markman* Hr'g. Tr. 5-6, Mar. 9, 2012.

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1   patent. *See* Declaration of Timothy J. Drabik ("Drabik Decl.") ¶ 17. The specification and the

2   claims make it clear that the decoder decodes digital video. For example, each of the claims at

3   issue refers to "an apparatus for decoding an encoded picture from a bitstream." Similarly, the

4   specification describes that "the decoder decodes the [encoded] pictures." '374 patent, 4:57-59.

5   As described in the specification, the general idea behind decoding is to "decompress" video data:

6   After the compressed video data has been transmitted, it must be decoded,
        or decompressed. In this process, the transmitted video data is processed

7   to generate approximation data that is substituted into the video data to
        replace the "non-essential" data that was removed in the coding process.

8   '374 patent, 1:62-67. Decoders are further discussed in the specification in the context of widely

9   known video coding standards:

10   Consequently, video coding standards have been developed to standardize
        the various video coding methods so that the compressed digital video

11   content is rendered in formats that a majority of video encoders and
        decoders can recognize.

12

13 '374 patent, 2:10-14. The specification identifies MPEG-1, MPEG-2, MPEG-4, H261 and H263

14 as examples of video coding standards in wide use. '374 patent, 2:9-19.   These uses of "decoder"

15 in the specification, in combination with the reference to well-known MPEG/ITU-T video coding

16 standards, connote to a person of ordinary skill in the art that the "decoder" referred to in the

17 specification is a discrete, well-known class of structures called digital video decoders. Drabik

18 Decl. ¶ 23.

19   Digital video decoder structures have well-known, basic components for decoding encoded

20 digital video content—entropy decoding, inverse scanning, inverse quantization, inverse transform

21 and prediction. Drabik Decl. ¶ 20. These components invert the processes used to encode the

22 video data: entropy decoding is the inverse of equally well-known entropy coding, inverse

23 scanning is the inverse of equally well-known scanning, inverse quantization is the inverse of

24 equally well-known quantization, inverse transform is the inverse of equally well-known

25 transform, and inverse prediction is the inverse of equally well-known prediction. *Id.*

26   The known class of digital video decoders is implemented using several types of electronic

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1 devices, including devices that use different technologies to implement the basic structural

2 components of the decoder. *Id.* at ¶ 24. The specification discloses that a "decoder" can be

3 implemented as a processor, ASIC, FPGA, CODEC, or DSP:

4
> The encoder or decoder can be a processor, application specific integrated
> circuit (ASIC), field programmable gate array (FPGA), coder/decoder
5 > (CODEC), digital signal processor (DSP), or some other electronic device
> that is capable of encoding the stream of pictures. . . .   The term
6 > "decoder" will be used to refer expansively to all electronic devices that
> decode digital video content comprising a stream of pictures.
7

8 '374 patent, 4:59-5:3. Each of these implementations, whether hardware or software, would have

9 the basic structural components for performing entropy decoding, inverse scanning, inverse

10 quantization, inverse transform, inverse prediction, and picture reconstruction. At the time of the

11 filing of the specification, digital video decoders implemented using ASICs (Drabik Decl. ¶¶ 28-

12 30), FPGAs (Drabik Decl. ¶¶ 31-32), or DSPs (Drabik Decl. ¶¶ 33-35) were known and

13 commercially available. In an ASIC implementation, the various structural components

14 correspond directly to hard-wired physical blocks of circuitry. Drabik Decl. ¶ 26. In an FPGA

15 implementation the structural components are configured through programming of connections

16 among circuit elements. *Id.* Once programmed, an FPGA possesses physical blocks of circuitry

17 corresponding to functional blocks, just as an ASIC does. *Id.* With respect to software

18 implementations on a processor or a DSP, the various structural components are defined by

19 procedures or software tasks, which control the operation of the computer or DSP structure,

20 through which video data is processed. *Id.*

21   Because the specification connotes to one of ordinary skill in the art a known class of

22 structures for performing the claimed functions, the requirements of 35 U.S.C § 112, ¶ 6 are

23 satisfied. The specification does not need to describe the routine details on how to build the

24 known structural components of a decoder. A person of ordinary skill in the art would have

25 understood from the disclosure in the specification how to implement the claimed functions in a

26 decoder. Drabik Decl. ¶¶ 49-52; *see Intel Corp.*, 319 F.3d at 1366, 1370 (holding that the internal

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1 circuitry of an electronic device need not be disclosed in the specification if one of ordinary skill

2 in the art would understand how to build and modify the device); *S3 Inc. v. Nvidia Corp.*, 259 F.3d

3 1364, 1370-71 (Fed. Cir. 2001) (holding that "selector" was structure for the "means . . . for

4 selectively receiving," and that "[t]he law is clear that patent documents need not include subject

5 matter that is known in the field of the invention and is in the prior art, for patents are written for

6 persons experienced in the field of the invention…. To hold otherwise would require every patent

7 document to include a technical treatise for the unskilled reader."); *Telcordia Techs., Inc. v. Cisco*

8 *Sys., Inc.*, 612 F.3d 1365, 1376-77 (Fed. Cir. 2010) (holding that "controller" was structure for

9 "monitoring means," and that "an ordinary artisan would have recognized the controller as an

10 electronic device with a known structure."); *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d

11 1316, 1338-39 (Fed. Cir. 2008) (holding that "video standard detector" was the structure for

12 "circuitry to provide format signal changeable in response to the format of said video type signal"

13 and that "the absence of internal circuitry in the written description does not automatically render

14 the claim indefinite."); *Atmel Corp.*, 198 F.3d at 1381 (holding that the title of the article in the

15 specification may, by itself, be sufficient to indicate to one skilled in the art the precise structure

16 of the means for performing the recited function); *Goss Int'l Ams., Inc. v. Graphic Mgmt. Assocs.*,

17 739 F. Supp. 2d 1089, 1100 (N.D. Ill. 2010) (holding that "controller" was the structure for

18 "control means" and that "a controller is a known structure that is a type of special purpose

19 computer…. these controllers may not even require any algorithms at all if they consist of only

20 circuitry to perform their specific purpose.").

21   Microsoft argues that the term "decoder" is used in the Motorola Patents in a functional

22 manner to describe all structures that have decoding functionality, and does not identify a specific

23 structure. DKT. 205 at 8. But, this ignores that it is sufficient if the specification identifies to one

24 of ordinary skill in the art a "class" of structures. *Linear Tech. Corp. v. Impala Linear Corp.*, 379

25 F.3d 1311, 1322 (Fed. Cir. 2004) ("That the disputed term is not limited to a single structure does

26 not disqualify it as a corresponding structure, as long as the class of structures is identifiable by a

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1   person of ordinary skill in the art."). A person of ordinary skill in the art would have understood

2   the term "decoder" to include the basic structural components common to the video coding

3   standards, which were developed to "standardize the various video coding methods so that the

4   compressed digital video content is rendered in formats that a majority of video encoders and

5   decoders can recognize." '374 patent, 2:11-14. Indeed, such decoders were both known and

6   commercially available. Drabik Decl. ¶¶ 28-38, 45-48. The decoder of the claimed inventions

7   modifies the prediction functions of the known decoder structure, and those modifications are

8   described in the specification. Drabik Decl. ¶¶ 49-52. One of ordinary skill, reading the

9   specification, would have known how to build and modify the known decoder structures to

10 perform the claimed functions. *Id.*; *see Intel Corp.*, 319 F.3d at 1366.

B.   The Case Law Requiring Disclosure of an Algorithm Does Not Apply in This Case to the Disclosure of a "Decoder."

13 Microsoft relies on cases, such as *Aristocrat Techs. Austl. PTY Ltd. v. Int'l Game Tech.*,

14 521 F.3d 1328 (Fed. Cir. 2008), for the proposition that patents that claim a computer-

15 implemented function in "means-plus-function" form must disclose an algorithm for performing

16 that function as part of the Section 112, ¶ 6 requirement to disclose corresponding structure. DKT.

17 205 at 7. These cases are completely inapposite.

18 As discussed in *Aristocrat*, the rationale for this requirement is that a general purpose

19 computer programmed to perform a particular function is in effect a special purpose computer, and

20 on that basis may be patented. *Aristrocrat*, 521 F.3d at 1333 (citing *WMS Gaming v. Int'l Gaming*

21 *Tech.*, 184 F.3d 13398 (Fed. Cir. 1999) and *In re Alappat*, 33 F.3d 1526 (Fed. Cir. 1994)). The

22 corollary is that a patent claiming a general purpose computer programmed to perform a function

23 must be limited to that special purpose computer structure (plus equivalents), and must disclose

24 the algorithm that defines it. However, where as here, a patent claims an apparatus that has

25 structures that are more particular and well known than that of a general purpose computer, such

26 as a known decoder structure, the rationale underlying these cases does not exist, and they should

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1   not apply.

2   Microsoft argues that "the common specification must disclose an algorithm to avoid

3   invalidity for indefiniteness" because the Motorola Patents "identify only general purpose

4   hardware as performing the 'decoding' function." DKT 205 at 10. However, as discussed above,

5   the Motorola Patents do not identify mere general purpose hardware as the structure for

6   performing the claimed functions. Instead, they disclose a "decoder," which is more than just a

7   general purpose computer. It was understood by one of ordinary skill to be a discrete class of

8   known structures. That this known structure could be implemented by using a processor does not

9   mean that the disclosed structure is just any general purpose computer. The disclosed structure is

10 limited to electronic devices having the structural components of a decoder as dictated by the

11 video coding standards with which it must comply, as modified to perform the claimed function.

12 Moreover, it was known to be so by those of ordinary skill in the art.

13   Thus, the cases relied on by Microsoft are inapplicable in this case because, unlike here,

14 the **only** structure identified for performing the claimed function in those cases was a

15 microprocessor or a general purpose computer that was not otherwise part of a known type of

16 device. *See WMS Gaming, Inc.*, 184 F.3d at 1349 ("the structure disclosed . . . is a *microprocessor*

17 programmed to perform the algorithm illustrated in Figure 6"); *Aristocrat*, 521 F.3d at 1334

18 (specification disclosed "any *standard microprocessor* base [sic] gaming machine"); *Net*

19 *MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1367 (Fed. Cir. 2008) (specification disclosed

20 "*general purpose bank computer*"); *HTC Corp. v. IP-Com GmBH & Co.*, 667 F.3d 1270, 1280

21 (Fed. Cir. 2012) (a processor and transceiver alone amount to "*nothing more than a general*

22 *purpose computer*"); *Dealertrack v. Huber*, Nos. 2009-1566, 2009-1588, 2012 WL 164439, at *12

23 (Fed. Cir. Jan. 20, 2012) ("[a] *general purpose computer* can perform the claimed function…");

24 *Timeline, Inc. v. ProClarity Corp.*, No. 05-1013, 2007 WL 1103092, at *5 (W.D. Wa. Apr. 11,

25 2007) ("the structure for performing the claimed function is a main process running on a

26 *computer*"); *In re Aoyama*, 656 F.3d 1293, 1298 (Fed Cir. 2011) (Figure 8 and corresponding

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1 description "fail[ed] 'to describe, even at a high level, how a *computer* could be programmed to

2 produce the structure that provides the results described in the boxes.'").

3 　　　　Citing to a sentence from the dissent, Microsoft argues that the Court in *Aoyama* "required

4 an algorithm for a means element corresponding to an ASIC or an FPGA." DKT. 205 at 5. To the

5 contrary, the majority opinion in that case did not discuss ASICs or FPGAs in connection with the

6 claimed function. Rather, the Court addressed whether a flowchart (Figure 8) linked to the

7 claimed function adequately disclosed structure for performing the claimed function. *Aoyama*,

8 656 F.3d at 1297. Paragraph 0019 of the specification to which Microsoft points for disclosure of

9 an ASIC and FPGA is a description of Figure 1 of the patent at issue, not of Figure 8. Thus,

10 Microsoft's representation that the Court "required an algorithm for a means element

11 corresponding to an ASIC or an FPGA" is incorrect.

12 　　　　**C.　　　Even If Disclosure of an Algorithm Is Required, the Specification Discloses
Algorithms for Performing the Claimed Functions.**

13

14 　　　　If this Court determines that the *Aristocrat* line of cases applies to the "means for

15 decoding" and "means for using" claim elements, one of ordinary skill in the art would understand

16 that the specification of the Motorola Patents discloses such an algorithm, operating within the

17 decoder structure, for performing each of the corresponding claimed functions.

18 　　　　In *Atmel*, the Federal Circuit explained the role of the specification in functional claiming

19 under § 112 ¶ 6:

20 　　　　All one needs to do in order to obtain the benefit of that claiming device is to recite
some structure corresponding to the means in the specification, as the statute

21 　　　　states, so that one can readily ascertain what the claim means and comply with the
particularity requirement of ¶ 2. The requirement of specific structure in § 112, ¶ 6

22 　　　　thus ***does not raise the specter of an unending disclosure of what everyone in the
field knows*** that such a requirement in § 112, ¶ 1 would entail.

23

24 *Atmel*, 198 F.3d at 1382. The Federal Circuit has applied this principle to the claiming of

25 computer implemented functions. *Typhoon Touch Techs.*, *Inc. v. Dell, Inc.*, 659 F.3d 1376, 1384

26 (Fed. Cir. 2011). In particular, the Federal Circuit has applied this principle in cases holding that

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1 sufficient algorithmic structure was disclosed in the specification. In *Typhoon*, the Federal Circuit

2 reversed a district court's determination that a means element was indefinite for failure to provide

3 an algorithm. *Id.* The means plus function limitation at issue was "means for cross-referencing

4 responses to said inquiries with possible responses from one of said libraries." *Id.* at 1379. The

5 specification disclosed that this means "entail[ed] the steps of data entry, then storage of data in

6 memory, then the search in a library of responses, then the determination if a match exists, and

7 then reporting action if a match is found." *Id.* at 1386. The Federal Circuit held that this was

8 sufficient, because "it suffices if the specification recites in prose the algorithm to be implemented

9 by the programmer" and the patentee "is not required to produce a listing of source code or a

10 highly detailed description of the algorithm to be used to achieve the claimed functions in order to

11 satisfy 35 U.S.C. § 112 ¶ 6." *Id.* at 1385-86.

12 In *AllVoice Computing PLC v. Nuance Commc'ns, Inc.*, 504 F.3d 1236, 1241-42 (Fed. Cir.

13 2007), the Federal Circuit reversed a district court's determination that a means element was

14 indefinite. The means plus function limitation at issue was "output means for outputting the

15 recognised words into at least any one of the plurality of different computer-related applications."

16 *Id.* at 1241. The specification disclosed that this means "us[ed] the dynamic data exchange

17 ('DDE') protocol in the Windows operating system." *Id.* The Federal Circuit held that this was

18 sufficient, because "a person of ordinary skill in this art would understand the DDE protocol," and

19 that "preparing the software instruction . . . would be a trivial matter well within the reach of a

20 person of ordinary skill in the art." *Id.* at 1242.

21 Like in *Typhoon* and *AllVoice*, the specification of the Motorola Patents discloses

22 algorithms for the decoder structure that would be understood by one of ordinary skill in the art as

23 performing the claimed functions. For each of the means elements, the specification of the

24 Motorola Patents discloses the algorithms in the form of methods, rules and prose. This is all that

25 the case law requires. *Typhoon*, 659 F.3d at 1385 ("[p]recedent and practice permit a patentee to

26 express that procedural algorithm 'in any understandable terms'"…[and the] "patent need only

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1   disclose sufficient structure for a person of skill in the field to provide an operative software

2   program for the specified function").

3   **1.**   **The Specification Discloses Algorithms for the Decoder Structure That Are Sufficient to Give Meaning to Each of the "Means for Decoding" Claim Elements.**

4

5   As discussed below, Motorola's proposed algorithm for each of the "means for decoding"

6   elements is supported by the specification and consistent with how a person of ordinary skill in the

7   art would understand the specification to disclose the algorithms that correspond to the claimed

8   functions.

9   **(a)**   **"means for decoding . . . in inter coding mode"**

Claim Term for Construction	Agreed Function	Agreed Structure	Algorithm
means for decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock, wherein at least one block within at least one of said plurality of smaller portions at a time is encoded in inter coding mode ('374	decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock	a decoder	Motorola: (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) performs inter prediction on blocks of the macroblock pairs in frame mode and field mode using at least one of the median, average, weighted average, "yes/no method," "always method," "selective method," "alt selective method," or "directional segmentation prediction
			Microsoft: in field mode, creating in memory one or more macroblocks each containing one field and one or more macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and in frame mode, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from

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Claim Term for Construction	Agreed Function	Agreed Structure	Algorithm
Patent, claim 14)			both fields

The parties agree that the claimed function for the "means for decoding . . ." element of the '374 patent, claim 14 is precisely as written in the claim. The parties also agree that the structure is a decoder.[2] The parties, however, disagree as to whether an algorithm is disclosed in the specification, and if so, what the algorithm consists of.

One of ordinary skill in the art would know and understand that there is an algorithm disclosed in the specification that corresponds to the claimed function. This algorithm enables a decoder to: (1) receive from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pair; and (2) perform inter prediction on blocks of the macroblock pairs in frame mode and field mode using at least one of the median, average, weighted average, "yes/no method," "always method," "selective method," "alt selective method," or "directional segmentation prediction." Drabik Decl. ¶ 59.

A person of ordinary skill in the art would have understood that the "means for decoding…in inter coding mode" element is directed to using inter prediction to decode pairs of macroblocks that are in frame mode or in field mode. The claim element refers specifically to "inter coding mode." Drabik Decl. ¶ 54. From the specification, the person of ordinary skill in the art knows and understands that the decoder receives in the bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs. '374 patent, 8:46-65, FIG. 7, FIG. 11; Drabik Decl. ¶ 55. He also knows and understands from the specification that the decoder performs inter prediction on blocks of the frame and field based macroblock pairs

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[2]   As discussed above, the parties' agreement as to "decoder" is subject to each party reserving its position as to whether structure is adequately disclosed in the specification.

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1 according to at least one of the inter prediction methods disclosed in the specification. '374

2 patent, 9:9-12:56 ("median," "average," "weighted average," "yes/no method," "always method,"

3 "selective method," "alt selective method," and "directional segmentation prediction"), Fig. 12,

4 Fig. 7, 7:50-53, 7:65-67; Drabik Decl. ¶ 55. He further knows and understands from the

5 specification that the various inter prediction methods disclosed in the specification are linked to

6 the claimed function of decoding macroblock pairs together in frame coding mode and field

7 coding mode. '374 patent, 9:46-59 (the blocks "can be in either frame or field mode"), 10:34-37

8 (referring to "macroblock pair based AFF"), 11:28-31 ("[t]his method can be used in . . . pair

9 based macroblock AFF . . . coding"), Drabik Decl. ¶ 57. This prosaic and pictorial description,

10 *Typhoon, supra,* is an adequate disclosure of the relevant algorithms. How to implement this

11 algorithm in software was well within the skill in the art. Drabik Decl. ¶ 60.

12 Microsoft argues that "frame/field decoding occurs after and to right of the 'inverse

13 prediction' block." DKT. 205 at 11. But, it is clear from the specification that prediction **is** a

14 frame/field decoding operation (where prediction is performed on blocks within macroblock pairs

15 in frame/field mode), **not** an operation that occurs after frame/field decoding. *See e.g.*, '374

16 patent, 15:64-65 ("In the case of decoding the prediction modes of blocks . . ."), 16:1-2 ("[I]n the

17 case of decoding the prediction modes of blocks . . ."), 16:4-5 ("In the case of decoding the

18 prediction mode of blocks . . ."), 16:6-7 ("In the case of decoding the prediction modes of the

19 block . . ."), 15:49-50 ("blocks . . . in frame or field mode"), 16:12-23, ("macroblock pair (170) is

20 decoded in field mode . . ."), 16:24-35 ("macroblock pair (170) is decoded in frame mode . . ."),

21 10:34-37 ("referring to "macroblock pair based AFF""), 11:29-31 ("[t]his method can be used in .

22 . . pair based macroblock AFF coding"); Drabik Decl.¶ 58.

23 As set forth above, Motorola has properly identified a sufficient algorithm performed in

24 the decoder structure corresponding to the claimed function. In light of the specification, "one

25 skilled in the art would understand the bounds of the claim," and the "means for decoding"

26 element should be held definite. Drabik Decl. ¶ 59; *see Personalized Media Commc'ns, LLC v.*

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1   *ITC*, 161 F.3d 696, 705 (Fed. Cir. 1998).

2   Microsoft disagrees with this identification of the algorithm.[3] Microsoft's proposed

3   identification is incorrect. Microsoft contends that the algorithm for the "means for decoding"

4   includes "processing" the field macroblocks "to create" frame macroblocks (containing lines from

5   both fields). However, this is not part of the "means for decoding." One of ordinary skill in the

6   art understands from the specification that reinterleaving the lines of the top and bottom field

7   macroblocks to create frame macroblocks occurs *after* the "decoding." Drabik Decl. ¶ 74. The

8   specification describes FIG. 8 in terms of how the encoder operates (i.e., from left to right):

9   if the pair of macroblocks (700) is to be encoded in field mode, it is **first split** into
       one top field 16 by 16 pixel block (800) and one bottom field 16 by 16 pixel block

10   (801), as shown in FIG. 8. The two fields are **then coded separately**.

11   '374 patent, 7:54-58. This shows that encoding happens after splitting the lines of the top and

12   bottom fields. The decoder simply operates in reverse—(i.e., from right to left) the top and

13   bottom field macroblocks depicted on the right in FIG. 8 are **first decoded** and **then**

14   **reinterleaved** (unsplit) to construct the pair of frame macroblocks depicted on the left of FIG. 8.

15   Drabik Decl. ¶ 74. As explained below, the reinterleaving of the field lines is part of the "means

16   for using" algorithm, not the "means for decoding."[4] Thus, Microsoft has the right idea—the

17   algorithm for decoding can be identified—but Microsoft just points to the wrong algorithm for the

18   decoder.

19   Accordingly, Motorola's algorithm for the "means for decoding . . . in inter coding mode"

20

21   [3]   Although Microsoft contends that the "means for decoding" claim elements are indefinite, it also manages to
propose a construction. Microsoft acknowledged in its claim construction brief that the algorithm for performing the

22   claimed function of the "means for decoding" elements is disclosed in the specification. *See* DKT. 173 at 12-16
("Microsoft's proposal properly tracks the **algorithm disclosed in the specification**") ("Microsoft properly identifies

23   the disclosed structure and the **algorithm disclosed in the specification** for performing the claimed function.").
Although its construction is incorrect, Microsoft's ability to propose that construction shows that the term is not

24   indefinite. The issue for the Court is really about which identification of the algorithm is correct.

25   [4]   Microsoft also contends that the algorithm for the "means for decoding" involves "removing [a] mode."
DKT. 173 at 8. However, as the specification explains, decoding processes operate "**in a mode.**" '374 patent, 16:12-
59 (explaining what happens if designated macroblock pairs are "decoded **in frame/field mode**"); *see also* DKT. 174

26   at 8.

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1   is consistent with the disclosure in the specification and should, therefore, be adopted, confirming

2   that this term is definite.

3   **(b)**   **"means for decoding . . . in intra coding mode at a time"**

Claim Term for Construction	Agreed Function	Agreed Structure	Algorithm
means for selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock, wherein at least one block within at least one of said plurality of smaller portions is encoded in intra coding mode at a time ('375 patent, claim 13)	selectively decoding at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode	a decoder	**Motorola**: (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) performs intra prediction on blocks of the macroblock pairs in at least one of the vertical, horizontal, DC prediction, diagonal down/left, diagonal down/right, vertical-left, horizontal-down, vertical-right, horizontal-up, or plane prediction modes, using neighboring blocks determined by at least one of Rule 1, Rule 2, Rule 3 or Rule 4 '374 patent, 15:52-16:63
			Microsoft: in field mode, creating in memory one or more macroblocks each containing one field and one or more macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and in frame mode, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from both fields

The analysis for the intra coding limitation is similar to that for the inter-coding limitation

discussed above. Here, the parties agree that the claimed function for the "means for selectively

decoding . . ." element of the '375 patent, claim 13 is precisely as written in the claim. The parties

also agree that the structure is a decoder.[5] The parties, however, disagree again as to whether an

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[5]   As discussed above, the parties' agreement as to "decoder" is subject to each party reserving its position as to whether structure is adequately disclosed in the specification.

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1   algorithm is disclosed in the specification, and if so, what the algorithm consists of.

2   As above, one of ordinary skill in the art would know and understand that there is an

3   algorithm disclosed prosaically and pictorially in the specification that corresponds to the claimed

4   function. The algorithm enables a decoder to: (1) receive from a bitstream information including

5   pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which

6   mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) perform intra

7   prediction on blocks of the macroblock pairs in at least one of the vertical, horizontal, DC

8   prediction, diagonal down/left, diagonal down/right, vertical-left, horizontal-down, vertical-right,

9   horizontal-up, or plane prediction modes, using neighboring blocks determined by at least one of

10 Rule 1, Rule 2, Rule 3 or Rule 4 at '374 patent, 15:52-16:63; Drabik Decl. ¶ 66.

11   A person of ordinary skill in the art would have understood that the "means for

12 decoding…in intra coding mode at a time" element is directed to using intra prediction to decode

13 pairs of macroblocks that are in frame mode or in field mode. Drabik Decl. ¶ 61. This claim

14 element refers specifically to "intra coding mode." Drabik Decl. ¶ 61. From the specification, the

15 person of ordinary skill in the art knows and understands that the decoder receives in the bitstream

16 information including pairs of macroblocks and a frame/field flag before each macroblock pair

17 that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs.

18 '374 patent, 8:46-65, FIG.7, FIG. 11; Drabik Decl. ¶ 62. He also knows and understands from the

19 specification that the decoder performs intra prediction on blocks of the frame based or field based

20 macroblock pairs in at least one of the vertical, horizontal, DC prediction, diagonal down/left,

21 diagonal down/right, vertical-left, horizontal-down, vertical-right, horizontal-up, or plane

22 prediction modes, using neighboring blocks determined by at least one of Rule 1, Rule 2, Rule 3

23 or Rule 4. '374 patent, 14:37-16:63, FIG. 14, FIG. 15, FIG. 16a-b, FIG. 17a-d; Drabik Decl. ¶ 62.

24 He further knows and understands from the specification that the various intra prediction methods

25 disclosed in the specification are linked to the claimed function of decoding macroblock pairs

26 together in frame coding mode and field coding mode. *See, e.g.*, '374 patent, 14:64-65 ("An intra

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1   block and its neighboring blocks may be coded in frame or field mode"), 15:48-49 ("Block C and

2   its neighboring blocks A and B can be in frame or field mode"), 15:64-65 ("In the case of

3   decoding the prediction modes of blocks . . ."), 16:12-23, ("If the above macroblock pair (170) is

4   decoded in field mode. . ."), 16:24-35 ("if the above macroblock pair (170) is decoded in frame

5   mode . . ."); Drabik Decl. ¶ 65. This prosaic and pictorial description, *Typhoon, supra,* is an

6   adequate disclosure of the relevant algorithms. How to implement this algorithm in software was

7   well within the skill in the art. Drabik Decl. ¶ 67.

8   　　　　As set forth above, Motorola has properly identified a sufficient algorithm performed in

9   the decoder structure corresponding to the intra-coding function. In light of the specification, "one

10 skilled in the art would understand the bounds of the claim," and the "means for decoding . . ."

11 element should be held definite.

12 　　　　In sum, the parties disagree over what the claimed algorithm consists of. Microsoft's

13 definition shows that Microsoft knows an algorithm for this function can be found prosaically and

14 pictorially in the specification—it just chooses the wrong algorithm. This disagreement parallels

15 that as discussed above in Section (1) and that analysis applies here as well. Motorola's proposed

16 algorithm for the "means for decoding. . . in intra-coding mode at a time" is consistent with the

17 disclosure in the specification and should, therefore, be adopted , confirming that this limitation is

18 indeed definite.

19 　　　　　　(c)　　　"means for decoding . . . in a horizontal scanning path or a
20 　　　　　　　　　　vertical scanning path"

21

Claim Term for Construction	Agreed Function	Agreed Structure	Algorithm
means for decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a	decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of	a decoder	**Motorola**: (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; (2) decodes the macroblock pairs of a picture from left to right and from top to bottom, as shown in FIG. 9 path 900, or from top to bottom and

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Claim Term for Construction	Agreed Function	Agreed Structure	Algorithm
group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode, wherein said decoding is performed in a horizontal scanning path or a vertical scanning path ('376 patent, claim 22)	macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode, wherein said decoding is performed in a horizontal scanning path or a vertical scanning path		from left to right, as shown in FIG. 9 path 901; and (3) within each frame macroblock pair decodes the top macroblock of the macroblock pair first, followed by the bottom macroblock, and within each field macroblock pair decodes the top field macroblock of the macroblock pair first, followed by the bottom field macroblock
			Microsoft: in field mode, creating in memory one or more macroblocks each containing one field and one or more macroblocks each containing the other field and processing each such macroblock together with the other macroblocks to create in memory at least two macroblocks containing lines from both fields and in frame mode, creating in memory one or more macroblocks each containing lines from both fields and processing each such macroblock together to create in memory at least two macroblocks containing lines from both fields

Once again, the parties agree that the claimed function for the "means for decoding . . ." element of the '376 patent, claim 22 is precisely as written in the claim. The parties also agree again that the structure is a decoder.[6] The parties, however, disagree as to whether an algorithm is disclosed in the specification, and if so, what the algorithm consists of.

Here again, for similar reasons, one of ordinary skill in the art would know and understand that there is an algorithm disclosed in the specification that corresponds to the claimed function. Here, the algorithm is slightly different—it enables a decoder to: (1) receive from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; (2)

---

[6]   As discussed above, the parties' agreement as to "decoder" is subject to each party reserving its position as to whether structure is adequately disclosed in the specification.

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decode the macroblock pairs of a picture from left to right and from top to bottom, as shown in FIG. 9 path 900, or from top to bottom and from left to right, as shown in FIG. 9 path 901; and (3) within each frame macroblock pair decode the top macroblock of the macroblock pair first, followed by the bottom macroblock, and within each field macroblock pair decode the top field macroblock of the macroblock pair first, followed by the bottom field macroblock. Drabik Decl. ¶ 72.

A person of ordinary skill in the art would have understood that the "means for decoding" element is directed to using a horizontal scanning path or a vertical scanning path to decode pairs of macroblocks. Drabik Decl. ¶ 68. This claim element refers specifically to a "horizontal scanning path" and a "vertical scanning path." Drabik Decl. ¶ 68. From the specification, the person of ordinary skill in the art knows and understands that the decoder receives in the bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs. '374 patent, 8:46-65, FIG. 7, FIG. 11; Drabik Decl. ¶ 69. He also knows and understands from the specification that the decoder decodes the macroblock pairs of a picture from left to right and from top to bottom, as shown in FIG. 9 path 900, or from top to bottom and from left to right, as shown in FIG. 9 path 901. '374 patent, FIG. 9, 7:44-48; Drabik Decl. ¶ 69. He further knows and understands from the specification that within each frame macroblock pair, the decoder decodes the top macroblock of the macroblock pair first, followed by the bottom macroblock; and within each field macroblock pair, the decoder decodes the top field macroblock of the macroblock pair first, followed by the bottom field macroblock. '374 patent, FIG. 9, 8:14-18; Drabik Decl. ¶ 69. This prosaic and pictorial description, *Typhoon, supra,* is an adequate disclosure of the relevant algorithms. How to implement this algorithm in software was well within the skill in the art. Drabik Decl. ¶ 73.

Motorola has properly identified a sufficient prosaic and pictorial algorithm performed in the decoder structure corresponding to the function. In light of the specification, "one skilled in

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1   the art would understand the bounds of the claim," and the "means for decoding . . ." element

2   should be held definite.

3   The parties disagree again over what the claimed algorithm consists of. This disagreement

4   parallels that as discussed above in Section (1) and that analysis applies here as well. Motorola's

5   proposed algorithm for the "means for decoding . . . in a horizontal scanning path or a vertical

6   scanning path" is consistent with the disclosure in the specification and should, therefore, be

7   adopted, confirming that this limitation is indeed definite.

8   **2.   The Specification Discloses an Algorithm for the Decoder Structure
              That Is Sufficient to Give Meaning to the "Means for Using" Claim**
9   **Elements.**

10

11

Claim Term for Construction	Agreed Function	Agreed Structure	Algorithm
means for using said plurality of decoded [smaller portions/processing blocks] to construct a decoded picture ('374 patent, claim 14, '375 patent, claim 13, '376 patent, claim 22)	using said plurality of decoded [smaller portions/processing blocks] to construct a decoded picture	a decoder	**Motorola**: (1) for a decoded frame macroblock pair, uses the frame macroblocks of the macroblock pair for the decoded picture; (2) for a decoded field macroblock pair, reinterleaves the top and bottom field lines of the macroblock pair to form frame macroblocks and uses the frame macroblocks of the macroblock pair for the decoded picture; and (3) for a frame or field macroblock pair in which a macroblock is skipped, uses a co-located macroblock in a reference picture for the decoded picture.
			Microsoft: assembling a decoded picture using the decoded [smaller portions/processing blocks] like bricks in a wall

20   The analysis for "means for using" parallels the analysis previously described for "means

21   for decoding". Here, the parties agree that the claimed function for the "means for using . . ."

22   elements is precisely as written in the claims. The parties also agree that the structure is a

23   "decoder."[7] The parties, however, disagree as to whether an algorithm is disclosed in the

24   specification, and if so, what the algorithm consists of.

25

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[7]   As discussed above, the parties' agreement as to "decoder" is subject to each party reserving its position as to
26   whether structure is adequately disclosed in the specification.

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One of ordinary skill in the art would know and understand that there is an algorithm disclosed in the specification that corresponds to the claimed function. The algorithm enables a decoder to: (1) for a decoded frame macroblock pair, use the frame macroblocks of the macroblock pair for the decoded picture; (2) for a decoded field macroblock pair, reinterleave the top and bottom field lines of the macroblock pair to form frame macroblocks and use the frame macroblocks of the macroblock pair for the decoded picture; and (3) for a frame or field macroblock pair in which a macroblock is skipped, use a co-located macroblock in a reference picture for the decoded picture. Drabik Decl. ¶ 77.

One of ordinary skill in the art would know and understand from the specification that there is an algorithm disclosed that corresponds to the function of using macroblock pairs to construct a decoded picture. Drabik Decl. ¶ 76. From the specification, the person of ordinary skill in the art knows and understands that for a decoded frame macroblock pair, the decoder uses the frame macroblocks for the decoded picture. *Id.* He understands that for a decoded field macroblock pair, the decoder reinterleaves the top and bottom field lines of the macroblock pair to form frame macroblocks and uses the frame macroblocks of the macroblock pair for the decoded picture. FIG. 8 illustrates to one of ordinary skill in the art that in the encoding direction (from left to right), the encoder splits the odd and even lines of the pair of frame macroblocks to form top and bottom field macroblocks; and that in the decoding direction (from right to left), the decoder reinterleaves the lines of the top and bottom field macroblocks to form the frame macroblocks and uses those frame macroblocks for the decoded picture. Drabik Decl. ¶ 76. The specification further describes that for a frame or field macroblock pair in which a macroblock is skipped, a co-located macroblock in a reference picture is used for the decoded picture during picture reconstruction. '374 patent, 12:67-13:5, 13:12-19, 14:21-28; Drabik Decl. ¶ 76. This prosaic and pictorial description, *Typhoon, supra,* is an adequate disclosure of the relevant algorithms. How to implement this algorithm in software was well within the skill in the art. Drabik Decl. ¶ 78.

Motorola has properly identified a sufficient algorithm performed in the decoder structure

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1   corresponding to the claimed function. In light of the specification, "one skilled in the art would

2   understand the bounds of the claim," and the "means for using" elements should be held definite.

3   As before, the parties also disagree over what the algorithm consists of.[8] Microsoft's

4   proposed construction is incorrect for at least the following reasons. First, Microsoft's

5   construction ignores that one of ordinary skill in the art understands from the specification that,

6   during picture reconstruction, the lines of the top and bottom field macroblocks of the macroblock

7   pair are reinterleaved into frame macroblocks prior to being added to the decoded picture. Drabik

8   Decl. ¶ 79. Second, Microsoft's construction is overly narrow. It seeks to limit the function

9   performed by the structure by adding that the structure perform[s] "the algorithm of assembling a

10 decoded picture using the decoded [smaller portion/processing blocks] like bricks in a wall."

11 DKT. 173at 19-20. This is improper because neither the claims nor the specification limit the

12 method of construction to be "assembly," "like bricks in a wall." The specification more broadly

13 discloses that the picture construction includes copying for skipped macroblocks. '374 patent,

14 12:67-13:5, 13:12-19, 14:21-28; Drabik Decl. ¶ 80. Motorola's proposed algorithm for the

15 "means for using" is consistent with the disclosure in the specification and should, therefore, be

16 adopted.

17   Plainly, the specification discloses, albeit in prose and pictures and not mathematical

18 formulae, algorithms that perform the claimed functions in the decoder. That is all that is required

19 by law and should put an end to this motion. Even if Microsoft quarrels with the adequacy of the

20 algorithms, that is a fact issue for a jury.

21 **IV.   CONCLUSION**

22   In summary, Microsoft's motion for summary judgment of invalidity should be denied

23 because it is unable to show by clear and convincing evidence that the claims at issue fail to

24

25

26

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1   satisfy the requirements of 35 U.S.C. § 112, ¶ 2 and § 112, ¶ 6.

2   DATED this 6th day of April, 2012.

3   Respectfully submitted,

4   SUMMIT LAW GROUP PLLC

5

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21

22

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24   ───────────────────────
      [8]   Although Microsoft contends that the "means for using" claim elements are indefinite, it also proposes a
25   construction. *See* DKT. 173 at 19-20. Although its construction is incorrect, Microsoft's ability to propose that
      construction shows that the term is not indefinite. The real issue for the Court is to determine which construction is
26   correct.

MOTOROLA'S OPPOSITION TO MICROSOFT'S
MOTION FOR SUMMARY JUDGMENT OF
INVALIDITY - 22
CASE NO. C10-1823-JLR

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MOTOROLA'S OPPOSITION TO MICROSOFT'S
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I hereby certify that on this day I electronically filed the foregoing with the Clerk of the Court using the CM/ECF system which will send notification of such filing to the following:

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MOTOROLA'S OPPOSITION TO MICROSOFT'S
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CASE NO. C10-1823-JLR

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